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Study of Temperature Dependent Ultra Low Power Deep Submicron Digital CMOS Logic

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Abstract—*The immense demand of low power portable applications such as cellular phones, bio-medical instruments and other communication devices led to the development of integrated circuits operating in subthreshold region of operation. Various circuits operating in subthreshold region are available in the literature and its performance at room temperature has been calculated and analyzed. Since, temperature is one of the major process variation parameter; the focus in this paper has been made to identify the various parameters of short channel MOSFET that are dependent on temperature. The identified parameters will be utilized to study the temperature dependent performance of basic digital CMOS gates operating in subthreshold region. The results of analytical model are verified with industry standard BSIM4. The error lies within the range of 15%.*

1. INTRODUCTION

Low power circuit design techniques such as voltage scaling and clock gating work well in the medium-power, medium performance region of the design spectrum, where the exquisite balance of power and delay is well maintained. [1] However, in the ultra-low power end of the design spectrum, where speed is of secondary importance, a more meticulous approach is warranted. Digital sub-threshold circuits have been proposed to meet the ultra-low power requirement [2][3]. By operating in the sub-threshold region, digital sub-threshold circuits utilize the continuously flowing leakage current as the switching current. However, the performance of the digital sub-threshold circuits is several orders of magnitude lower than their normal strong-inversion [4]. Hence, sub-threshold circuits are applicable to only specific applications where ultra-low power is of primary importance. Such applications range from the implantable pace-makers and defibrillators to the recently emerging wearable, wrist-watch computers and hear aid machine [5][6].

A sub-threshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current. While deriving drain current I_{ds}, it was assumed that the current flow is due to drift only. This resulted in I_{ds} =0 for gate to source voltage V_{gs}, less than threshold voltage V_{th} (V_{gs}<V_{th}) that is, there is no current flow for V_{gs} below threshold. In reality, this is not true and I_{ds} has small but finite value for V_{gs}<V_{th}. This current below V_{th} is called the sub-threshold or weak inversion current and occurs when $V_{gs} < V_{th}$. This minute leakage current, however, limits the maximum performance at which the sub-threshold circuit can be operated. Sub-threshold CMOS logic is the conventional CMOS logic operated in the sub-threshold region [7][8]. To ensure that the entire circuit is operating in the sub-threshold region, a supply voltage less than the threshold voltage of the transistor is used to power the circuit. In the sub-threshold region, therefore, due to the absence of conducting inversion channels, transistors behave differently as compared to when they are operated in a normal strong inversion region.

2. MOSFET MODEL IN SUBTHRESHOLD REGION

In subthreshold region of operation, the surface potential ϕ_s, is nearly constant from the source to the drain end because the inversion charge density $Q_i(y)$ is several orders of magnitude smaller than the bulk charge density Q_b.[11]

$$I_{ds1} = -\mu_s W Q_i(y) \frac{d\phi_s}{dy} \quad \text{Drift component} \qquad (1)$$

The surface potential ϕ_s is replaced by the ϕ_{ss} in subthreshold region. This shows that ϕ_{ss} is nearly linearly dependent on V_{gs}. Because ϕ_{ss} is constant, the electric field is zero. Hence, the only current that can flow is diffusion current.

$$I_{ds2} = \mu_s W V_t \frac{dQ_i(y)}{dy} \quad \text{Diffusion component} \qquad (2)$$

But according to the basic threshold model, the transistor is turned off, and there is no current flowing between drain and source when V_{gs}<V_{th}. But a more precise model considers the effect of thermal energy on the Boltzmann distribution which allows some of the more energetic electrons at the source to enter the channel and flow to the drain. This is also called the leakage current because transistor is off in this condition. In a sub-threshold the drain current is an exponential function of gate–source voltage and drain-source voltage.[5] The

subthreshold region of operation in MOSFET compare to strong region is shown in figure1. The symbol of NMOS is shown in fig. 2.

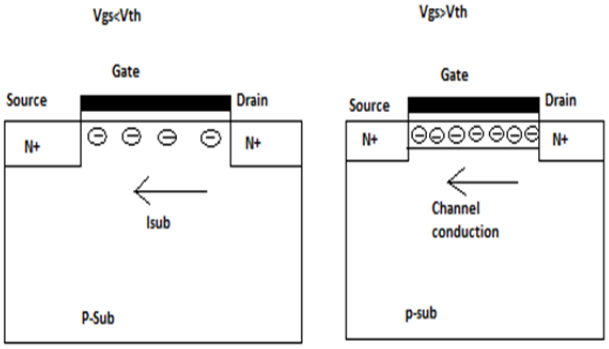

Fig. 1: Subthreshold region of operation in MOSFET

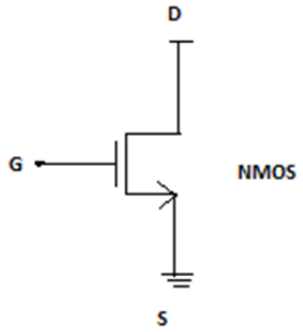

Fig. 2: NMOS transistor

In subthreshold region of operation, drain current is given as [1]

$$I_{dsub} = I_0 e^{\left(\frac{V_{gs}-V_t}{n\phi_t}\right)}\left(1 - e^{\frac{-V_{ds}}{\phi_t}}\right) ; V_{ds}<3\phi_t \quad (3)$$

$$I_{dsub} = I_0 e^{\left(\frac{V_{gs}-V_t}{n\phi_t}\right)} ; V_{ds}>3\phi_t \quad (4)$$

where I_0 represents drain current when $V_{gs}=V_t$ and is given by

$$I_0 = \mu_0 cox\left(\frac{w}{l}\right)(n-1)\phi_t \text{ when } V_{gs}=V_t \quad (5)$$

Where u_o is the carrier mobility, cox= eox/tox is the gate oxide capacitance (eox is the dielectric constant and tox is the gate oxide thickness), W and L are channel width and length, V_t is the threshold voltage, ϕ_t=kt/q is the thermal voltage and n=1+Cd/Cox is the sub-threshold slope factor.

When $V_{ds}<3\phi_t$ the drain current I_{dsub} does not depend upon the drain to source voltage and this is known as the saturation region of operation. When $0<=V_{ds}<=3\phi_t$ the drain current is exponentially depend upon the drain to source voltage and this known as the non saturation region.[9][3] The I-V characteristics of n-channel MOSFET operating in subthreshold region of operation is shown in fig. 3.

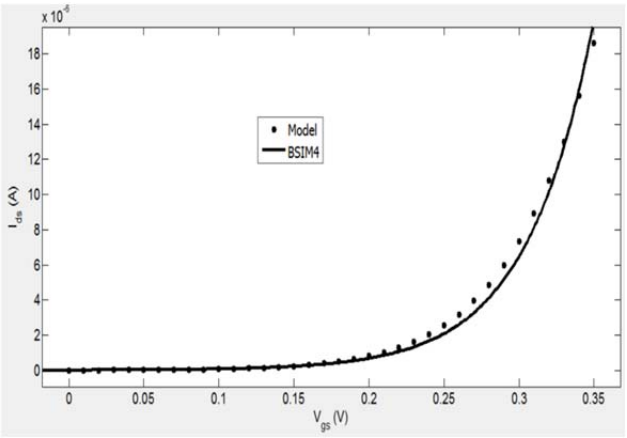

Fig. 3. I-V characteristics of n-channel MOSFET operating in subthreshold region of operation for 90nm technology node. V_{dd}=0.35V, V_{th}=0.399V

PMOS is built with p-type source and drain and n-type substrate. PMOS, carriers are holes. When a high voltage is applied to the gate, PMOS will not conduct. When a low voltage is applied in the gate, PMOS will conduct. PMOS represents P type MOS transistor. The drain current of the PMOS transistor, I_{dp}, can be found by replacing V_{gs} by V_{sg}, V_{ds} by V_{sd}, I_{0n} by I_{0p}, $(W/L)_n$ by $(W/L)_p$, n_n by n_p, and V_{thn} by $|V_{thp}|$. [7]

3. TEMPERATURE DEPENDENT PARAMETERS

3.1. Carrier mobility

Carrier mobility has very important relationship with temperature. Its dependency on temperature is dominated by two factors phonon scattering and ionized impurity scattering. Carrier mobility is defined as how fast the electron or hole moves through the semiconductor when pulled by the electric field. As temperature increases, thermal vibrations within a semiconductor increase and cause increased scattering. This causes the decrease in carrier mobility.[4][5]

$$\mu = \frac{e}{m}\tau \quad (6)$$

τ is the mean free time between the collision. And the mean free path is define as

$$\iota \approx \tau T^{1/2} \quad (7)$$

Now we have mean free path which is inversely proportional to the e scattering probability, and that the scattering

probability may be taken to be proportional to the energy of the lattice (T). So τ to be written as

$$\tau_{thermal} \approx \iota T^{-1/2} \approx T^{-3/2} \quad (8)$$

We therefore expect this decrease in the mobility to be proportional to $T^{-3/2}$. The effect of ionized impurity scattering, however, decreases with increasing temperature due to the average thermal speeds of the carriers being higher.

3.2. Saturation velocity

Saturation velocity is defined as maximum velocity of the charge carrier attain in the presence of high electric field. In the short channel devices the saturation velocity becomes the most important factor in performance. The relation between the temperature and saturation velocity is [4]

$$V_{sat} = \frac{V_{sat(300k)}}{(1-A_v) + A_v\left(T/300k\right)} \quad (9)$$

$V_{sat(300k)}$ = saturation velocity at 300k temperature. A_v= temperature coefficient for various devices.

In the above relationship the saturation velocity is inversely proportional to the temperature. In addition to temperature, the saturation velocity is also strongly depending upon the impurities and lattice defects.

3.3. Threshold voltage

Subthreshold region threshold voltage is define as the maximum voltage at which transistor starts operating.[10]

$$V_{tsub} = V_t - 4.605\left(n\frac{kT}{q}\right) \quad (10)$$

In the above equation V_t is expressed as

$$V_t = V_{FB} + \frac{1}{C_i}\sqrt{4\varepsilon_S qN_A\phi_f} + 2\phi_f \quad (11)$$

$$\frac{dV_T}{dT} = \frac{d\phi_f}{dT}\left(2 + \frac{1}{C_i}\sqrt{\frac{\varepsilon_s qN_A}{\phi_f}}\right) \quad (12)$$

$$\frac{d\phi_f}{dT} = \pm\frac{1}{T}\left[\frac{E_g(T=0K)}{2q} - \phi_f(T)\right] \quad (13)$$

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_A}{Ni}\right) \quad (14)$$

From the above equations, we find out that threshold voltage increase with decrease in temperature.

4. TEMPERATURE EFFECT ON THE PERFORMANCE OF THE SUBTHRESHOLD DEVICE CHARACTERISTICS

The circuit which is operating in subthreshold region, V_t, V_{gs} and V_{ds} are exponentially depend upon the drain current. And the dependency of temperature is also exponential so for designing of robust ultra low power devices the PVT become very important factor. Unlike strong inversion region the high overdrive gate voltage is applied, dominates the carrier mobility and the drain current in this region decrease with the increase in temperature, in subthreshold the drain current increase exponentially with temperature.[2]

So the drain current equation in subthreshold region with respect to temperature is

$$I_{dsub} = \mu_0 cox\left(\frac{w}{l}\right)(n-1)\phi_t^2 e^{\left(\frac{(V_{gs}-V_t)q}{nkT}\right)}\left(1 - e^{\frac{(-V_{ds})q}{kT}}\right) \quad (15)$$

From the above equation, show us the dependency of temperature with subthreshold drain current. In this region we find that due to increase in temperature the threshold voltage is decrease, because of the carrier mobility is also decrease down. The threshold voltage in this region has inverse relation with the supply voltage, if we increase the supply voltage the threshold voltage is decreases. And decrease in threshold voltage the subthreshold drain current (I_{dsub}) increases rapidly.[9]

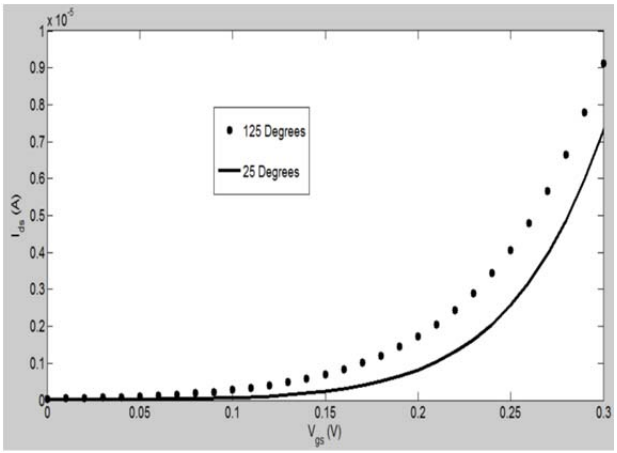

Fig. 4. I-V characteristics of n-channel MOSFET operating in subthreshold region of operation for 90nm technology node at two different temperatures. Vdd=0.35V, Vth=0.399V

5. CMOS INVERTER DC ANALYSIS

Sub-threshold CMOS logic operates with the power supply V_{dd} less than the transistors' threshold voltage V_t. This is done to ensure that all the transistors are indeed operating in the sub-threshold region.[2]

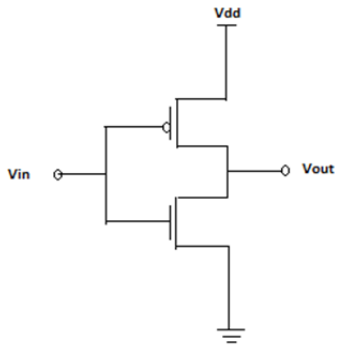

Fig. 5: CMOS inverter

The threshold voltage of CMOS inverter, both the PMOS and NMOS threshold voltage i.e. $|V_{thp}|$ and V_{thn} are considered to be V_t. In subthreshold region of operation the V_{dd} should be less then V_{th} i.e. the range lies between $3\phi_t<V_{dd}<V_t$.

The threshold voltage (V_{tsub}) in subthreshold region can define as voltage V_{gs} at which the drain current is equal to $0.01I_0$. Therefore equation (1) become [1]

$$0.01I_0 = I_0 e^{\left(\frac{V_{gs}-V_t}{n\phi_t}\right)}\left(1-e^{\frac{-V_{ds}}{\phi_t}}\right) \tag{16}$$

And after solving the above equation we get the result $V_{tsub}=V_t - 4.605(n\phi_t)$

From the above equation we have the region of operation of CMOS inverter in subthreshold region i.e. $V_t - 4.605(n\phi_t) < V_{ddsub} < V_t$

5.1. Temperature Effect on Voltage transfer characteristics (VTC) of CMOS inverter

Voltage transfer characteristics are something which gives us the relationship between the input voltages and output voltages. In this we apply the input voltages of certain amplitude and then determine the output voltage. Analytical expression of the VTC is determined by equating the NMOS and PMOS transistor current with each other. Put $I_{dn}=I_{dp}$ then, we have [6]

$$I_{ON}e^{\left(\frac{v_{gs}-v_{thn}(t)}{n_n kT/q}\right)}[1-e^{\frac{(-v_{ds})q}{kT}}]=I_{OP}e^{\left(\frac{v_{sg}-|v_{thp}|(t)}{n_n kT/q}\right)}[1-e^{\frac{(-v_{sd})q}{kT}}] \tag{17}$$

In the above equation I_{ON} is given by

$$I_{ON} = \mu_{on}(t)cox\left(\frac{w}{l}\right)_n (n_n - 1)\phi_t^2 \tag{18}$$

where μ_{on} is the electron mobility, Cox is the gate-oxide capacitance per unit area, W is the channel width, l is the channel length, V_{thn} is the threshold voltage, ϕ_t is the thermal voltage. The drain current of the PMOS transistor, I_{dp}, can be found by replacing V_{gs} by V_{sg}, V_{ds} by V_{sd}, I_{ON} by I_{OP}, $(W/L)_n$ by $(W/L)_p$, n_n by n_p, and V_{thn} by $|V_{thp}|$.

Now we have assume the $n_n=n_p$ (to obtain similar subthreshold slopes for the NMOS and PMOS devices) and put $V_{gs}=V_{in}$, $V_{ds}=V_{out}$, $V_{sg}=V_{dd}-V_{in}$ and $V_{sd}=V_{dd}-V_{out}$ results in,

$$I_{ON}e^{\left(\frac{v_{in}-v_{thn}(t)}{n_n kT/q}\right)}[1-e^{\frac{(-v_{out})q}{kT}}]=I_{OP}e^{\left(\frac{v_{sg}-v_{in}-|v_{thp}|(t)}{n_p kT/q}\right)}[1-e^{\frac{-(v_{sd}-v_{out})q}{kT}}] \tag{19}$$

Separating the v_{in} and v_{out} result in,

$$\frac{1-e^{\frac{-(v_{dd}-v_{out})q}{kT}}}{1-e^{\frac{(-v_{out})q}{kT}}} = \frac{I_{ON}}{I_{OP}}e^{\left(\frac{2v_{in}-v_{dd}-v_{thn}(t)-|v_{thp}|(t)}{n_n kT/q}\right)} \tag{20}$$

To simplify the analysis, let us investigate the above result for the following regions i.e. $v_{out}<<v_{dd}$ and $v_{out}=v_{dd}$.

For $v_{out}<<v_{dd}$ region, we have also assume [6]

$$1-e^{\frac{-(v_{dd}-v_{out})q}{kT}} \approx 1-e^{\frac{(-v_{dd})q}{kT}} \approx 1 \tag{21}$$

After simplifying the mathematical expression we have v_{out} equal to

$$v_{out} = \frac{kT}{q}\ln\frac{1}{1-\frac{I_{OP}}{I_{ON}}e^{-\left(\frac{2v_{in}-v_{dd}-v_{thn}(t)+|v_{thp}|(t)}{n_n kT/q}\right)}} \tag{22}$$

From above equation the value of v_{in} is

$$v_{in} = \frac{v_{dd}+v_{thn}(t)-|v_{thp}|(t)}{2} + n_n\frac{kT}{q}\ln\sqrt{\frac{I_{OP}}{I_{ON}}} \tag{23}$$

But the problem is that from this equation output voltage approaches to infinity which does not make sense. On the other case $v_{out}=v_{dd}$ and assume

$$1-e^{\frac{-(v_{out})q}{kT}} \approx 1-e^{\frac{(-v_{dd})q}{kT}} \approx 1 \tag{24}$$

After substituting these assumptions we get v_{out} equals to

$$v_{out} = v_{dd} - \frac{kT}{q}\ln\frac{1}{1-\frac{I_{ON}}{I_{OP}}e^{-\left(\frac{2v_{in}-v_{dd}-v_{thn}(t)+|v_{thp}|(t)}{n_n kT/q}\right)}} \tag{25}$$

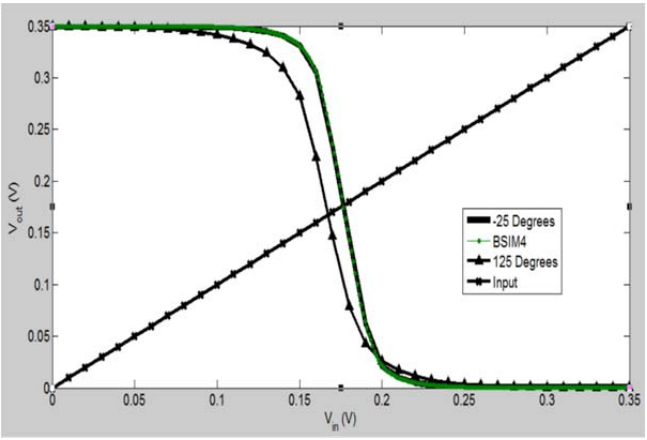

Fig. 6: Voltage transfer characteristics (VTC) of symmetric CMOS inverter operating in subthreshold region at 90nm technology node, v_{dd}=0.35V

6. CONCLUSION

The analytical model characterizing the MOSFET operating in subthreshold region of operation is discussed. It has been shown in the paper that how leakage current can be utilized to operate MOSFET at ultra low power. Since temperature is one of the most important process variation parameter, the effect of increase in temperature on the device dc characteristics and basic CMOS inverter voltage transfer characteristics has been studied. The results obtained are verified from industry standard BSIM4 and the error lies within the acceptable range of 5-10%.

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